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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,738	07/24/2003	Suguru Tachibana	107337-00049	8058

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ARENT FOX KINTNER PLOTKIN & KAHN
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,738	TACHIBANA ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the analog switch including a circuit for setting a potential of a gate of the first p-channel MOSFET to a potential of negative power supply voltage or ground potential; and for setting the potential of the gate to a potential lower than the potential of the negative power supply voltage or the ground potential as recited in claims 5-8 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: throughout the specification, "n MOS" and "p MOS" should be changed to –NMOS-- and --PMOS--, respectively. Also, on line 15 of page 13, "thepotential" should be changed to --the potential--. Note that the translated specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Objections

3. Claims 1-8 are objected to because of the following informalities:

In claim 1, line 1, "analog signal" should be changed to --analog input signal--.

In claim 1, line 6, it is suggested that "therefore which are" be changed to --therefore said first n-channel and first p-channel MOS field effect transistors are--.

Claim 1, line 7, it appears that "inputting an analog" should be changed to --receiving the analog--.

Claim 1, line 9, it appears that "inputting" should be changed to --receiving--.

Claim 1, line 16, "potential being" should be changed to --potential of the analog input signal being--.

Claim 1, line 20, "potential being" should be changed to --potential of the analog input signal being--.

Claim 1, line 22, "a" should be changed to --the--.

Claim 2, line 4, "a" should be changed to --the--.

Claim 3, line 2, it appears that "inputting" should be changed to --receiving--.

Claim 3, line 3, "the voltage boost" should be changed to --the boosting the potential of the gate of the first n-channel MOS field effect transistor to the potential higher than the potential of the positive power supply voltage--.

Claim 4, line 2, it appears that "inputting" should be changed to --receiving--.

Claim 4, line 3, "the voltage boost" should be changed to --the boosting the potential of the gate of the first n-channel MOS field effect transistor to the potential higher than the potential of the positive power supply voltage--.

In claim 5, line 1, "analog signal" should be changed to --analog input signal--.

In claim 5, line 6, it is suggested that "therefore which are" be changed to --therefore said first n-channel and first p-channel MOS field effect transistors are--.

Claim 5, line 7, it appears that "inputting an analog" should be changed to --receiving the analog--.

Claim 5, line 9, it appears that "inputting" should be changed to --receiving--.

Claim 5, line 16, "potential being" should be changed to --potential of the analog input signal being--.

Claim 5, line 20, "potential being" should be changed to --potential of the analog input signal being--.

Claim 5, line 22, "a" should be changed to --the--.

Claim 6, line 4, "a" should be changed to --the--.

Claim 7, line 2, it appears that "inputting" should be changed to --receiving--.

Claim 8, line 2, it appears that "inputting" should be changed to --receiving--.

Appropriate correction to the above informalities is required. Note that the above changes are needed so that the claims are clear.

Allowable Subject Matter

4. Claims 1-8 would be allowed if amended to overcome the above informalities.

Claim 1 would be allowed because the prior art of record fails to disclose or suggest an analog switch which includes all of the limitation of this claim. In particularly, the prior art of record fails to disclose or suggest the analog switch including a circuit for setting a potential of a gate of the first n-channel MOSFET to a potential of positive power supply voltage when the

potential of the input signal is lower than the potential of the reference signal, and for setting the potential of the gate to a potential higher than the positive power supply voltage when the potential of the input signal is higher than the potential of the reference signal.

Claims 2-4 are allowed because they depend on claim 1.

Claim 5 would be allowed because the prior art of record fails to disclose or suggest an analog switch which includes all of the limitation of this claim. In particularly, the prior art of record fails to disclose or suggest the analog switch including a circuit for setting a potential of a gate of the first p-channel MOSFET to a potential of negative power supply voltage (or ground potential) when the potential of the input signal is higher than the potential of the reference signal, and for setting the potential of the gate to a potential lower than the negative power supply voltage (or ground potential) when the potential of the input signal is lower than the potential of the reference signal.

Claims 6-8 are allowed because they depend on claim 5.

Conclusion

5. This application is in condition for allowance except for the above formal matters.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 15, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816